

Lab Manual:  
Communications Principles  
  
Using the EMONA Communications board for NI ELVIS III



Lab 12: Quadrature Phase Shift Keying (QPSK)

List of Updates

|  |  |
| --- | --- |
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# Lab 12: Quadrature Phase Shift Keying (QPSK)

## Learning Objectives

After completing this lab, you should be able to complete the following activities.

1. Examine the operation of a Serial to Parallel converter and v/v
2. Generate real BPSK and QPSK signals
3. Describe a QPSK signal in time and frequency domain
4. Explain the use of product detector demodulation in BPSK and QPSK
5. View QPSK as constellation, including phase delays

## Prerequisites

You should have completed Lab 1 and Lab 2 and be familiar with the equipment, its use and the handling precautions for the equipment.

## Required Tools and Technology

|  |  |
| --- | --- |
| Platform: NI ELVIS III Instruments used in this lab:   * Oscilloscope-Time * Oscilloscope-FFT | * Access instruments <https://measurementslive.ni.com> * View User Manual <http://www.ni.com/en-us/support/model.ni-elvis-iii.html> * View tutorials <https://www.youtube.com/playlist?list=PLvcPIuVaUMIWm8ziaSxv0gwtshBA2dh_M> |
| Hardware: Emona Communications Board Components used in this lab:   * Four BNC to 2mm banana-plug leads * Assorted 2mm banana-plug patch leads * Set of headphones or earbuds | * View User Manual <http://www.ni.com/en-us/support/model.emona-communications-board-for-ni-elvis-iii.html> |
| Software: LabVIEW Version 18.0 or Later  Toolkits and Modules:   * LabVIEW Real-Time Module * LabVIEW FPGA Module * NI ELVIS III Toolkit   Files used in this lab:  ECB\_EYE\_BER\_CONSTELLATION viewer\_LV2018 | * Before downloading and installing software, refer to your professor or lab manager for information on your lab’s software licenses and infrastructure * Download & Install for NI ELVIS III   <http://www.ni.com/academic/download>   * View Tutorials   <http://www.ni.com/academic/students/learn-labview/> |

## Expected Deliverables

In this lab, you will collect the following deliverables:

* Calculations
* Data from measurements
* Observations

Your instructor may expect you complete a lab report. Refer to your instructor for specific requirements or templates.

## Section 1: QPSK modulation

## 1.1 Theory and Background

As its name implies, *quadrature phase shift keying* (QPSK) is a variation of binary phase shift keying (BPSK). Recall that BPSK is basically a DSBSC modulation scheme with digital information for the message. Importantly though, the digital information is sent at a symbol rate of one bit at a time. QPSK is a DSBSC modulation scheme also but it sends has a symbol rate of two bits at a time (without the use of another carrier frequency).

As QPSK sends two bits of data at a time, it’s tempting to think that QPSK is twice as fast as BPSK but this is not so. Converting the digital data from a series of individual bits to a series of bit-pairs necessarily halves the data’s bit-rate. This cancels the speed advantage of sending two bits at a time.

So why bother with QPSK? Well, halving the data bit rate does have one significant advantage. The amount of the radio-frequency spectrum required to transmit QPSK reliably is half that required for BPSK signals. This in turn makes room for more users on the channel.

Figure 1 shows the block diagram of the mathematical implementation of QPSK.



Figure 1: Block diagram for QPSK modulation

At the input to the modulator, the digital data’s even bits (that is, bits 0, 2, 4 and so on)

are stripped from the data stream by a “bit-splitter” and are multiplied with a carrier to generate a BPSK signal (called PSKI). At the same time, the data’s odd bits (that is, bits 1, 3, 5 and so on) are stripped from the data stream and are multiplied with the same carrier to generate a second BPSK signal (called PSKQ). However, the PSKQ signal’s carrier is phase-shifted by 90° before being modulated. This is the secret to QPSK operation.

This “even/odd” labelling is somewhat arbitrary however is useful for our purposes of maintaining track of each bit stream.

The two BPSK signals are then simply added together for transmission and, as they have the same carrier frequency, they occupy the same portion of the radio-frequency spectrum. While this suggests that the two sets of signals would be irretrievably mixed, the required 90º of phase separation between the carriers allows the sidebands to be separated by the receiver using phase discrimination (introduced in Experiment 7). Figure 2 shows the block diagram of the mathematical implementation of QPSK demodulation.



Figure 2: Block diagram of full QPSK demodulation

Notice the arrangement uses two product detectors to simultaneously demodulate the two BPSK signals. This simultaneously recovers the pairs of bits in the original data. The two signals are cleaned-up using a comparator or some other signal conditioner then the bits are put back in order using a 2-bit parallel-to-serial converter.

To understand how each detector picks out only one of the BPSK signals and not both of them, recall that the product detection of DSBSC signals is “phase sensitive”. That is, recovery of the message is optimal if the transmitted and local carriers are in phase with each another. But the recovered message is attenuated if the two carriers are not exactly in phase. Importantly, if the phase error is 90º the amplitude of the recovered message is zero. In other words, the message is completely rejected (this issue is discussed in Section 3 of this lab).

The QPSK demodulator takes advantage of this fact. Notice that the product detectors in Figure 2 share the carrier but one of them is phase shifted 90°. That being the case, once the phase of the local carrier for one of the product detectors matches the phase of the transmission carrier for one of the BPSK signals, there is automatically a 90º phase error between that detector’s local carrier and the transmission carrier of the other BPSK signal. So, the detector recovers the data on the BPSK signal that it’s matched to and rejects the other BPSK signal.

## 1.2 Implement: Generating a QPSK signal

For this experiment you’ll use the ECB to generate a QPSK signal by implementing the mathematical model of QPSK. Once generated, you’ll examine the QPSK signal using the scope. Then, you’ll examine how phase discrimination using a product detector can be used to pick-out the data on one BPSK signal or the other.

It should take you about 1 hour to complete this experiment.

**1.3 Powering up the ELVIS III + EMONA Communications Board**

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| 1. | Ensure that the NI ELVIS III Application Board power button at the top left corner of the unit is OFF (not illuminated). |

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| --- | --- |
| 2. | Carefully plug the Emona Communications board (ECB) into the NI ELVIS III ensuring that it is fully engaged both front and back. |

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| --- | --- |
| 3. | Ensure that you have connected the NI ELVIS III to the PC using the USB cable and that the PC is turned on. |

|  |  |
| --- | --- |
| 4. | Turn on the Application Board *Power* button by pressing it once and confirm that it is illuminated. The LEDs on the ECB should also be illuminated. If they are not, then switch the unit off immediately and check for connection or insertion errors. |

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| --- | --- |
| 5. | Open the Instrument Launcher software in your browser and open the Scope. |

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| --- | --- |
| 6. | Configure the Scope with the settings found in the Scope Configuration table below. |

Scope Configuration

|  |  |
| --- | --- |
| Channels | CH1: Volts per division: 2V  CH2: Volts per division: 2V |
| Horizontal & Acquisition | Time per division: 2ms |
| Trigger | Digital edge, Source: TRIG, Slope: Rising |

|  |  |
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| 7. | Connect the set-up shown in Figure 3. Make sure that the micro-switch found under the EX-OR GATE module is set to *P2S*. Doing so sets the PARALLEL SERIAL/MUX module to Parallel-to-Serial mode.  **Note:** Insert the black plugs of the oscilloscope leads into a ground (*GND*) socket. |

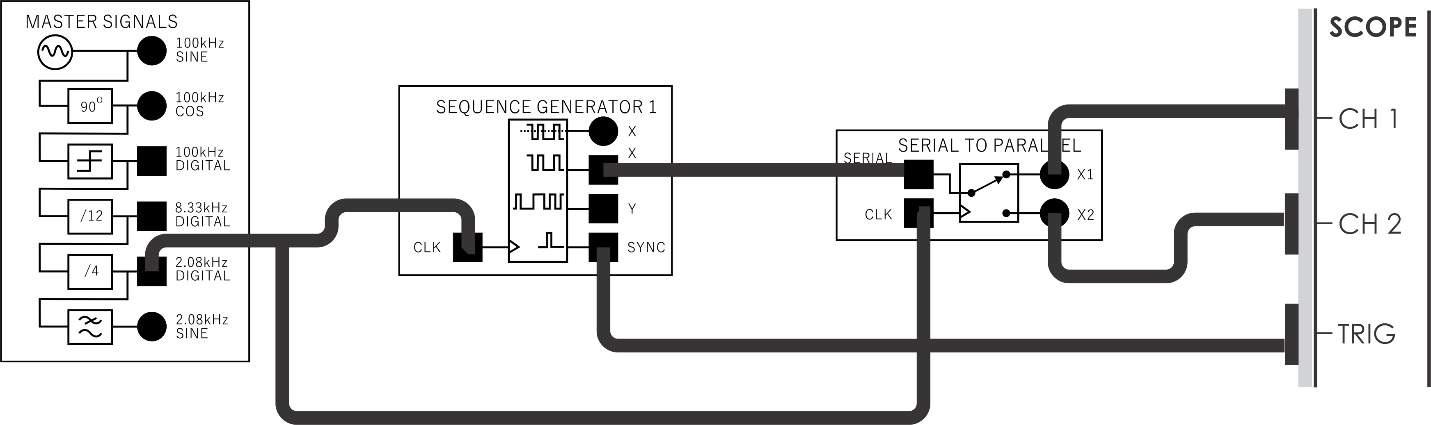


Figure 3: Patching for data bit splitting

This set-up can be represented by the block diagram in Figure 5. The Sequence Generator 1 module is used to model digital data with a symbol rate of 2.08kb/sec because it is clocked by the 2.08kHz Digital signal available on the Master Signals module. The 2-bit Serial-to-Parallel Converter module is used to split the stream of data bits from the Sequence Generator 1 module *X* sequence up into two streams of even bits and odd bits each at half of the rate of the input sequence.

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| --- | --- |
| 8. | Activate the scope’s CH 1 and CH 2 inputs to observe the Serial-to-Parallel Converter module *X1* and *X2* outputs. |

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| 9. | Pause the Scope and compare the signals. You should see two digital signals output from the Serial-to-Parallel Converter module that are different from each other.  **Optional:** Determine the symbol rate of the Serial-to-Parallel Converter module *X1* output by pausing the Scope and using the Scope vertical cursors to measure the period of a bit on either of the Scope channels. See Figure 4 for a hint. |

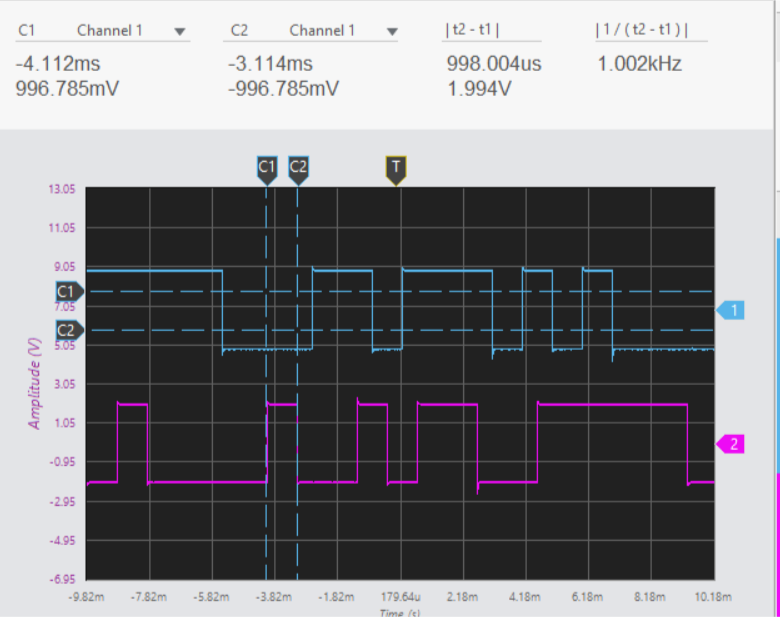
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Figure 4: Measurement of the BPSK bit rate using the Scope cursors

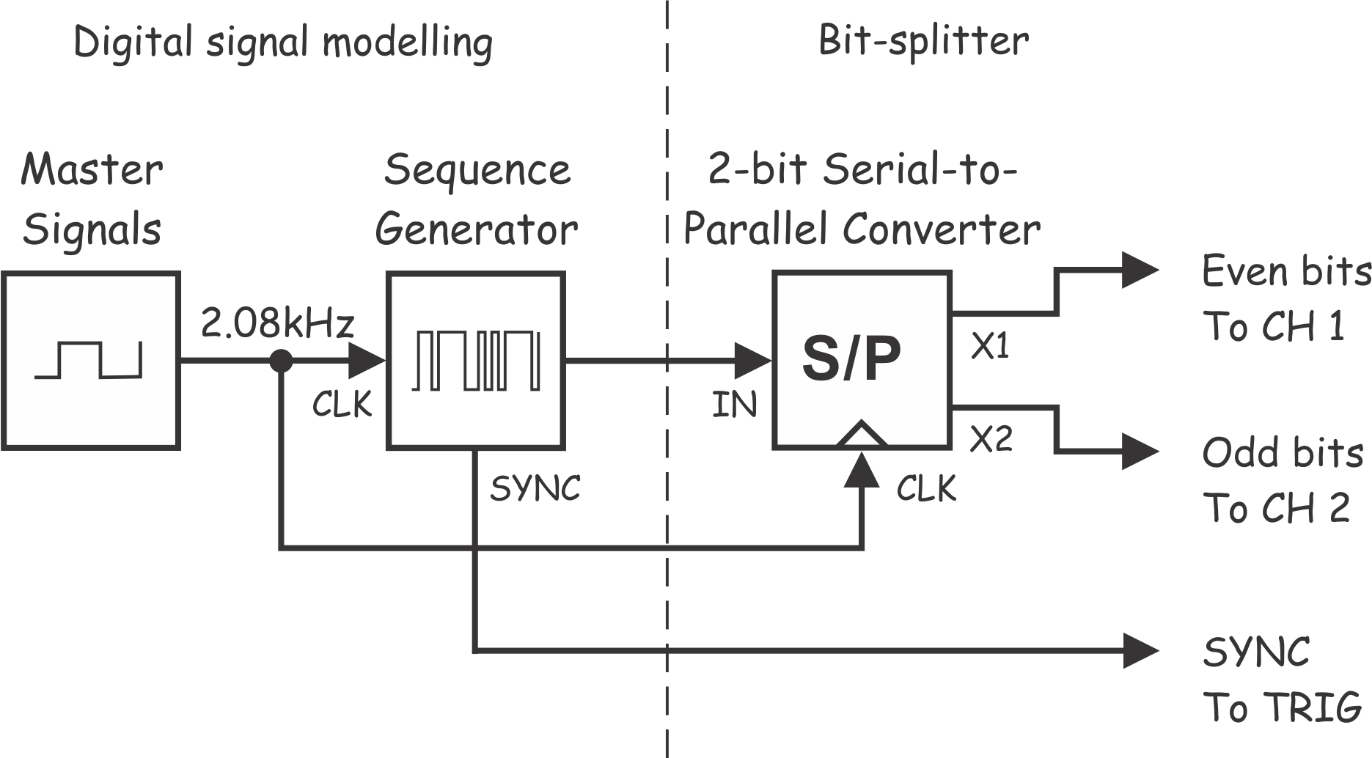


Figure 5: Block diagram for bit splitting

1-1 What is the relationship between the bit rate of the two digital signals output from the Serial-to-Parallel Converter and the bit rate of the Sequence Generator 1 module *X* output? **Tip:** If you’re not sure, see the preliminary discussion.

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| 10. | Modify the set-up as shown in Figure 6 .  Remember: Dotted lines show leads already in place. |

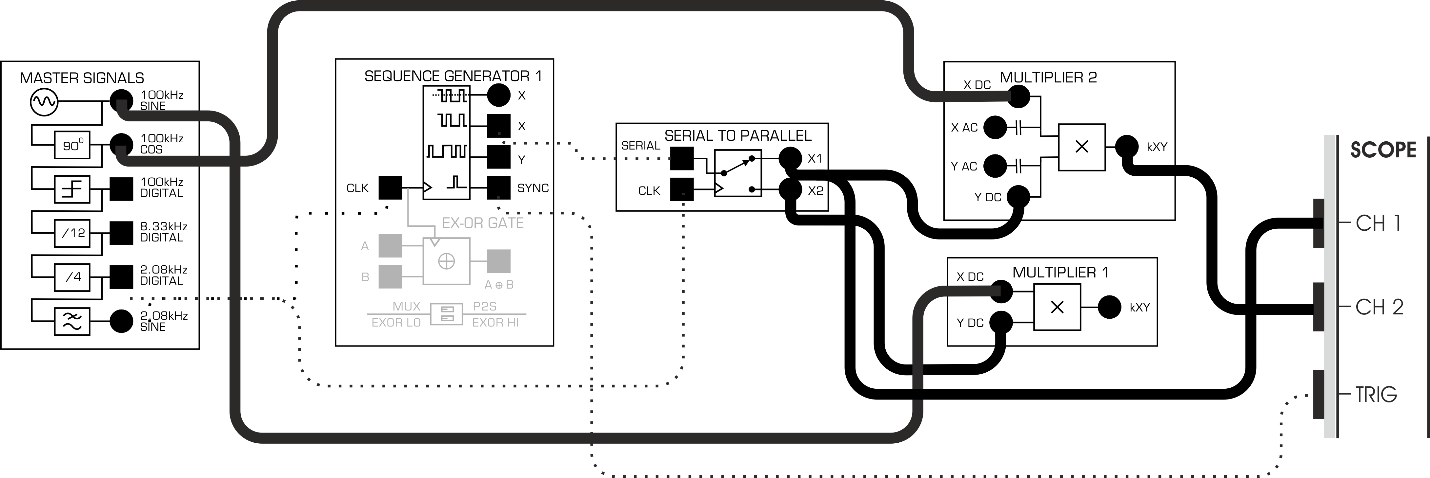


Figure 6: Patching for dual BPSK generation while examining the PSKI signal

Excluding the digital data modelling, this set-up can be represented by the block diagram in Figure 7. Notice that the bit-splitter’s two outputs are connected to independent Multiplier modules. The other input to the Multiplier modules is a 100kHz sinewave. However, the 100kHz signals are out of phase with each other by 90° which is a requirement of QPSK.

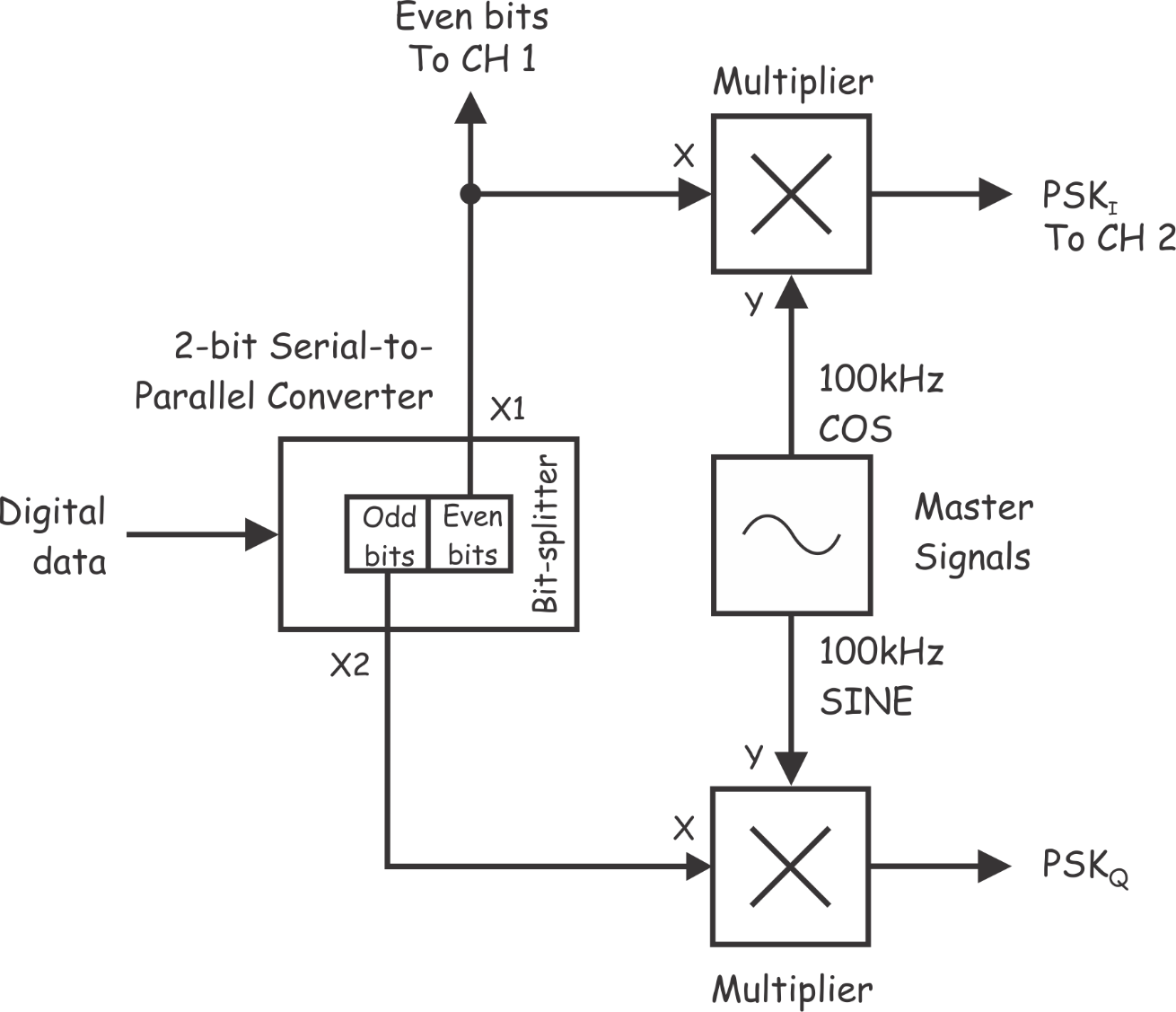


Figure 7: Block diagram for dual BPSK generation while examining the PSKI signal

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| --- | --- |
| 11. | Set the Scope Time per division setting to *200µs*. |

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| 12. | Compare the even data bits with the Multiplier module’s output (PSKI). |

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| 13. | Set the Scope Time per division setting *50µs*. |

|  |  |
| --- | --- |
| 14. | Examine the PSKI signal and look closely at the way it changes at the transitions in the even bit stream. |

1-2 What feature of the Multiplier 2’s output (PSKI) suggests that it’s a BPSK signal?

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| 15. | Move the scope’s connections as shown in Figure 8. |

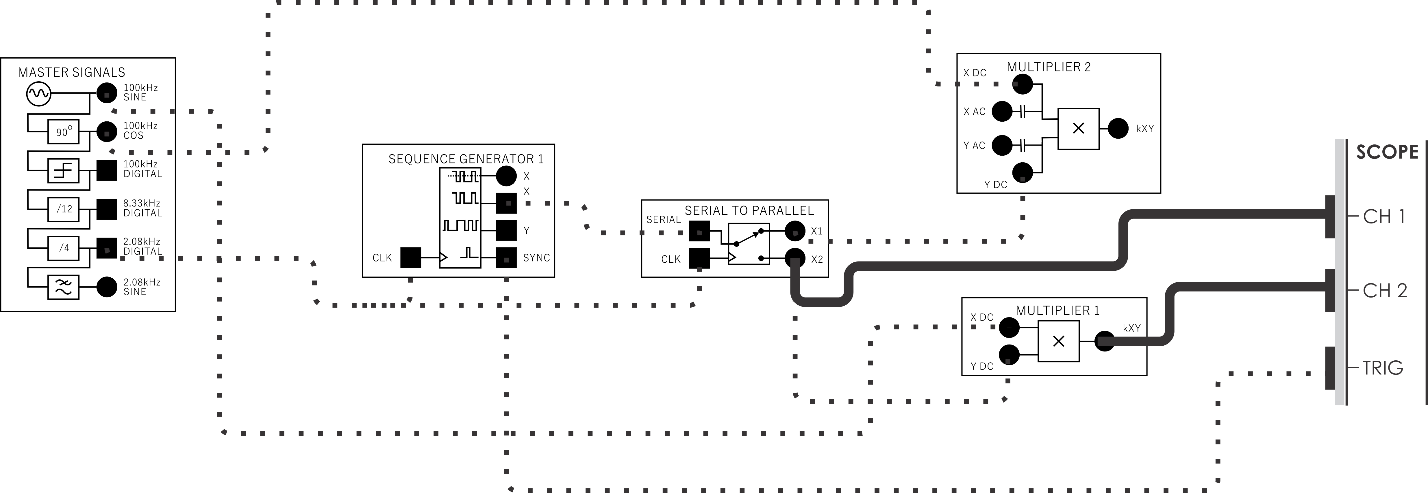


Figure 8: Patching for dual BPSK generation while examining the PSKQ signal

This change can be shown on the block diagram in Figure 9.

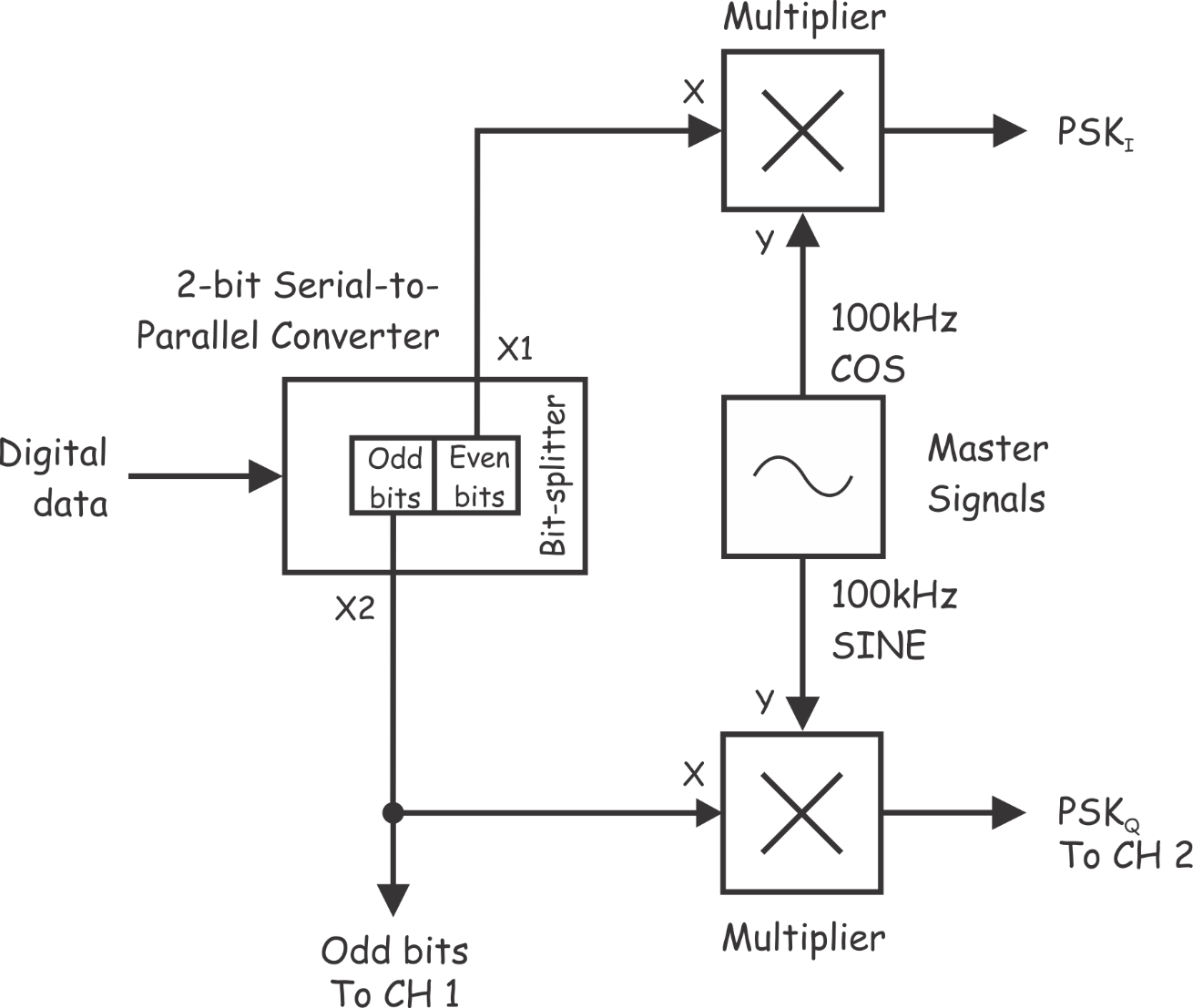


Figure 9: Block diagram for dual BPSK generation while examining the PSKQ signal

|  |  |
| --- | --- |
| 16. | Set the Scope Time per division setting to *200µs*. |

|  |  |
| --- | --- |
| 17. | Compare the odd bits of data with the Multiplier module’s output (PSKQ). |

|  |  |
| --- | --- |
| 18. | Set the Scope Time per division setting to *50µs*. |

|  |  |
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| 19. | Examine the PSKQ signal and look closely at the way it changes at the transitions in the odd bit stream. |

1-3 What type of signal is present on the Multiplier 1’s output?

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| 20. | Return the Scope Time per division setting to *100µs*. |

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| 21. | Modify the set-up as shown in Figure 10. |

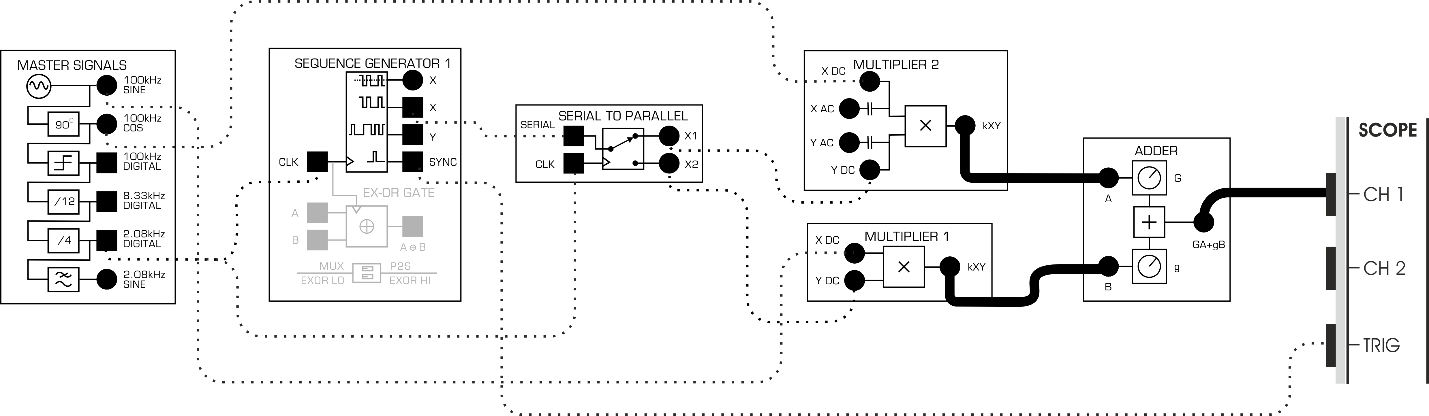


Figure 10: Patching for addition of dual BPSK channels

This set-up can be represented by the block diagram in Figure 11. The Adder module adds the PSKI and PSKQ signals. This turns the set-up into a complete QPSK modulator. The next several steps balance the gains on the Adder module to ensure that the PSKI and PSKQ contribute equally to the QPSK signal.

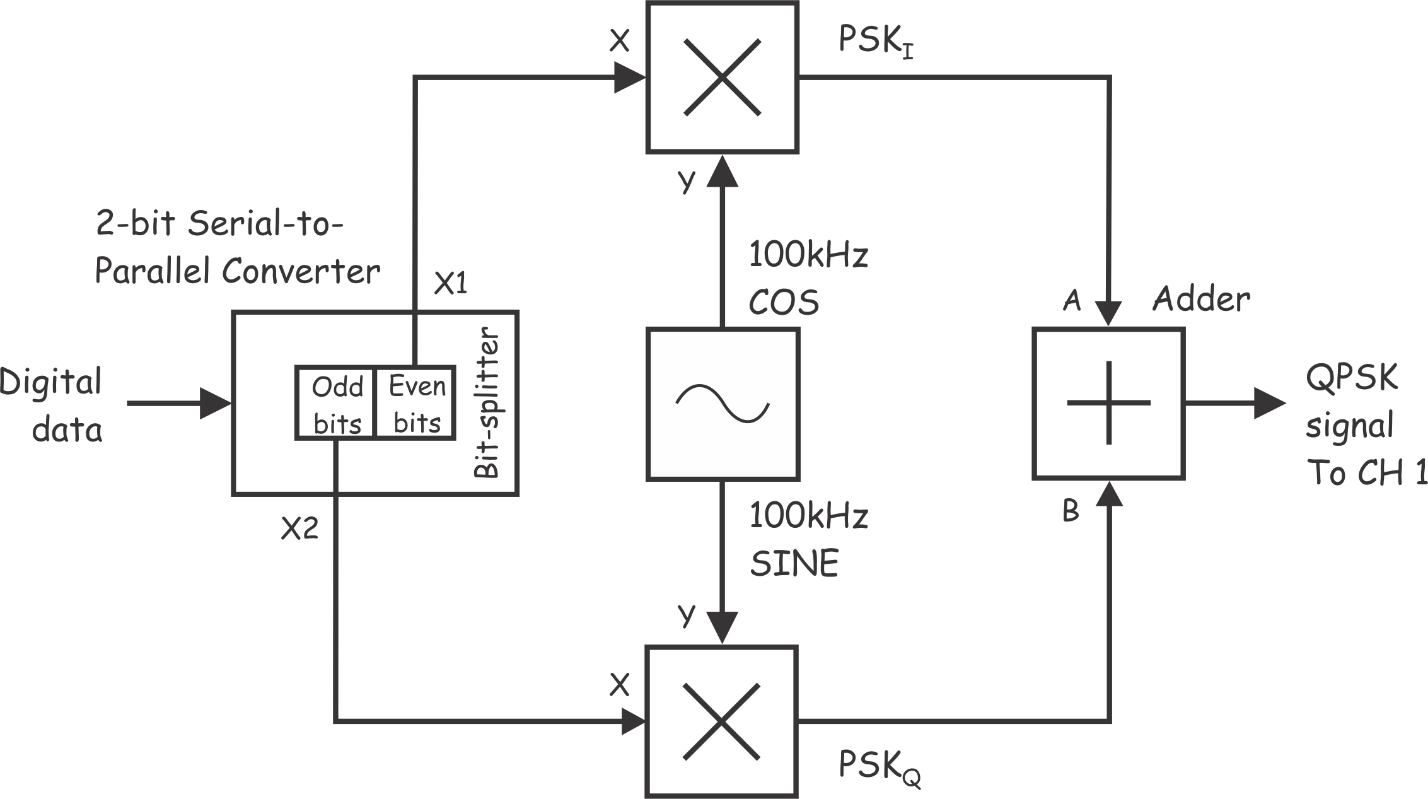


Figure 11: Block diagram for QPSK generation

|  |  |
| --- | --- |
| 22. | Disconnect the patch lead to the Adder module’s *A* input.  **Note:** This removes the BPSKI signal from the signal on the Adder module’s output. |

|  |  |
| --- | --- |
| 23. | Adjust the Adder module’s g knob to obtain a 4Vp-p output on Scope CH 1. |

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| 24. | Reconnect the patch lead to the Adder module’s *A* input. |

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| 25. | Disconnect the patch lead to the Adder module’s *B* input.  **Note:** This removes the BPSKQ signal from the signal on the Adder module’s output. |

|  |  |
| --- | --- |
| 26. | Adjust the Adder module’s *G* knob to obtain a 4Vp-p output on Scope CH 1. |

|  |  |
| --- | --- |
| 27. | Reconnect the patch lead to the Adder module’s *B* input. |

1-4 According to the theory, what type of digital signal transmission is now present on the Adder module’s output?

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|  | QPSK or OQPSK: What’s the difference?  QPSK modulation is normally generated from a single data stream converted to two parallel data streams. In this particular experiment, the serial/parallel converter outputs the parallel streams such that the bits are offset from each other by one clock period. Therefore, in this experiment we are actually implementing a form of QPSK known as *Offset QPSK* (OQPSK). |  |
|  |  |  |

## Section 2: Observations of QPSK bandwidth in the frequency domain

One of the advantages of QPSK over BPSK is its higher symbol rate for the same bandwidth. The next part of the experiment lets you see this for yourself using the Scope FFT display.

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| --- | --- |
| 1. | Configure the Scope as follows: |

Scope Configuration

|  |  |
| --- | --- |
| Channels | CH1: Volts per division: 2V |
| Horizontal & Acquisition | Time per division: 5ms |
| Trigger | Digital edge, Source: TRIG, Slope: Rising |
| Additional Channels | FFT: Enabled, Window: Hamming, Source: Channel 1 |

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| 2. | Set the Scope FFT Channel *Stop Frequency* parameter to 105kHz and set the Scope FFT Channel *Start Frequency* parameter to 95kHz. Doing so allows you to examine the 95kHz – 105kHz portion of the spectrum closely. |

|  |  |
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| 3. | Note the width of the main lobe centered at 100kHz, this is the bandwidth of the QPSK signal. |

2-1 What is the width of the main lobe centered at 100kHz for this **QPSK** signal?

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| 4. | Disconnect the Scope CH1 lead from the Adder module output and connect it to the Multiplier 2 module’s *kXY* input.  **Note:** You are now examining the BPSKI signal. |

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| 5. | Once again, note the width of the main lobe centered at 100kHz, this is the bandwidth of the BPSK signal. |

2-2 What is the width of the main lobe centered at 100kHz for this **BPSK** signal?

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2-3 What is the ratio of the width of the main lobe and the symbol rate for this **BPSK** signal?

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2-4 What is the ratio of the width of the main lobe and the symbol rate for this **QPSK** signal?

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## Section 3: Using phase discrimination to pick out one of the QPSK signal’s BPSK signals

It is interesting to demonstrate how phase discrimination is used by a QPSK demodulator to pick-out one or other of the two BPSK signals that make up the QPSK signal. The next part of the experiment lets you do this.

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| --- | --- |
| 1. | Locate the Phase Shifter module on the ECB and set its knob to about the middle of its travel. |

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| --- | --- |
| 2. | Locate the Amplifier & Headphone Output module on the ECB and set its *GAIN* knob to fully counterclockwise. |

|  |  |
| --- | --- |
| 3. | Locate the RRC FILTER 3 module on the ECB and set its *GAIN* knob to fully counterclockwise. Set its *TUNE* knob to fully clockwise. |

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| 4. | Modify the set-up as shown in Figure 12.  **Note:** As there are a lot of connections, you may find it helpful to tick them off as you add them. |

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| 5. | Connect Scope CH 1 to the output of the Amplifier & Headphone Output module and examine the Channel 1 *Volts Peak – Peak* value on the Scope Measurements display. Turn the Amplifier & Headphone Output module *GAIN* knob to set the *Volts Peak – Peak* to about 6V. |

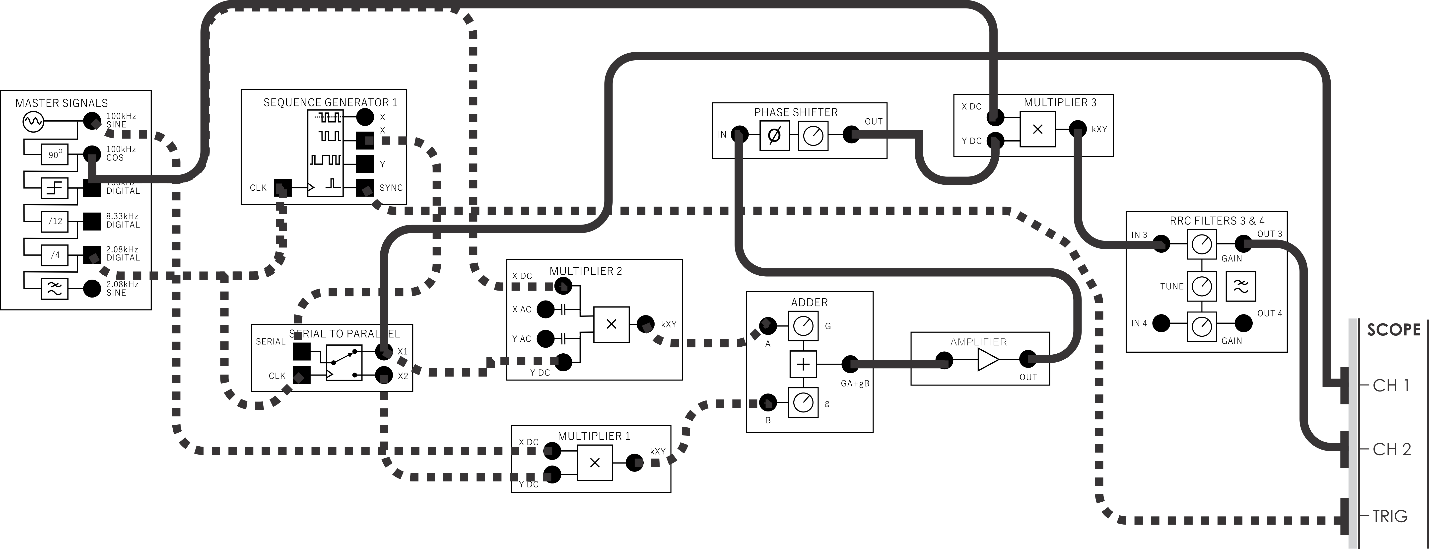


Figure 12: Patching for demodulation of the PSKI channel

The setup in Figure 12 can be represented by the block diagram in Figure 13. If you compare Figure 13 to Figure 2 in the preliminary discussion, you’ll notice that it implements a product detector consisting of a multiplier (mixer) and a low-pass filter. This setup is most of one arm of a QPSK demodulator (either I or Q). Ordinarily, the carrier would be generated locally (i.e. at the receiver) but they have been “stolen” from the modulator so that the pairs of carriers are synchronised which is a necessary requirement for QPSK demodulation.

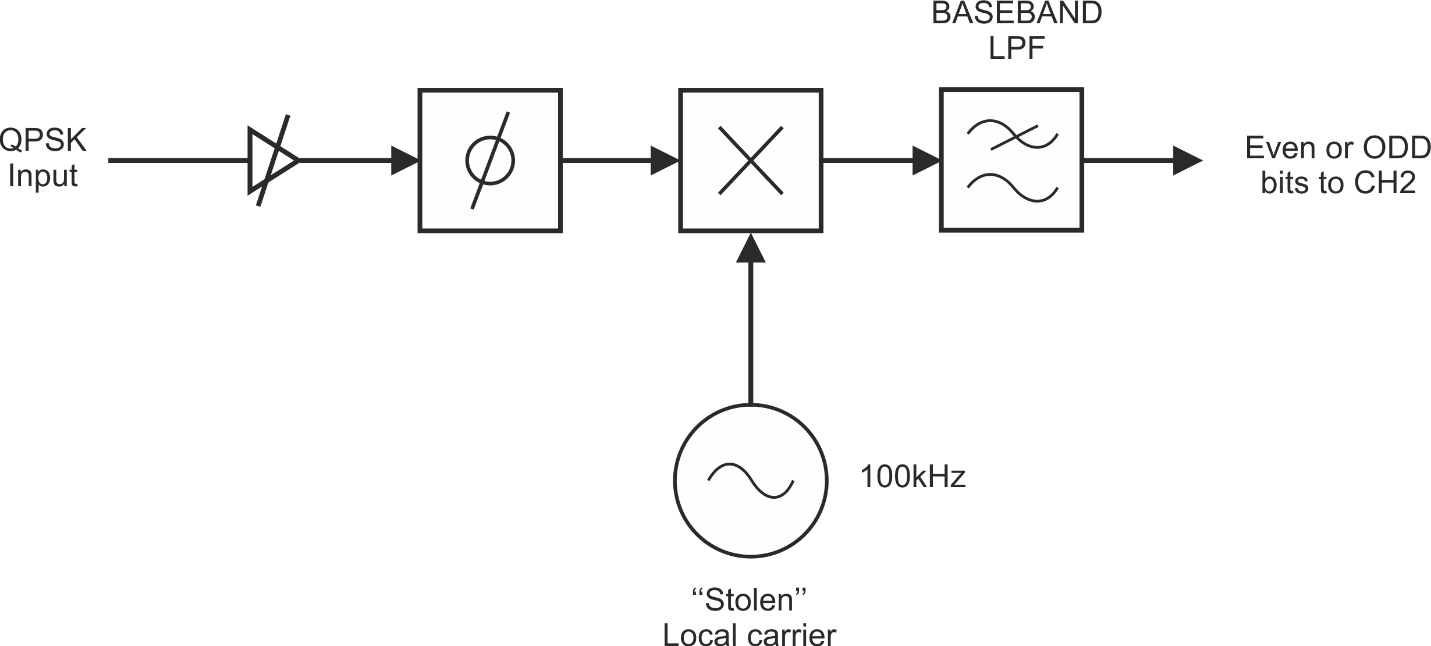


Figure 13: Block diagram for demodulation of one BPSK channel

|  |  |
| --- | --- |
| 6. | Connect Scope CH 1 to the Serial-to-Parallel Converter module’s *X1* output. Connect Scope CH 2 to the RRC Filter 3 module output. |

This setup uses the RRC Filter 3 module as the low-pass filter (LPF) required for the product detector. When the RRC Filter 3 module’s *FREQ* knob is turned fully clockwise, it has a cutoff frequency of about 14kHz which is sufficient to attenuate the high-frequency signal components that result from having multiplied (mixed) the signal with the 100kHz carrier while at the same time retaining a significant amount of the baseband signals harmonics.

As the set-up has not yet been “tuned”, the signal on the LPF’s (RRC FILTER 3) output likely consists of two quadrature components. Ordinarily, the phase of the local carriers is varied (while maintaining their 90° phase separation) to correct for the phase delay in the channel until only one opposing quadrature component appears on each LPF output. As the local carriers (and the bit-clock) have been stolen from the QPSK modulator in this case, this adjustment is modelled by varying the phase delay in the channel instead.

The Phase Shifter module and the Amplifier module are used to implement the adjustable phase delay in the channel. The Amplifier module inserts a 180o phase shift and the Phase Shifter module can be adjusted to implement a shift of up to 150o.

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| 7. | Compare the even data bits on the Serial-to-Parallel Converter module’s *X1* output with the demodulated data on the output of the RRC Filter 3 module. |

|  |  |
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| 8. | Vary the Phase Shifter module’s knob left and right and observe the effect on the demodulated signal. |

3-1 Why does the recovered signal have 3 or 4 voltage levels instead of 2 levels as you would expect for a digital signal?

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In the next part of this experiment, we will add a Comparator to the output of the RRC FILTER 3 module to clean up the output and create a digital signal.

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| 9. | Modify the set-up as shown in Figure 14. |

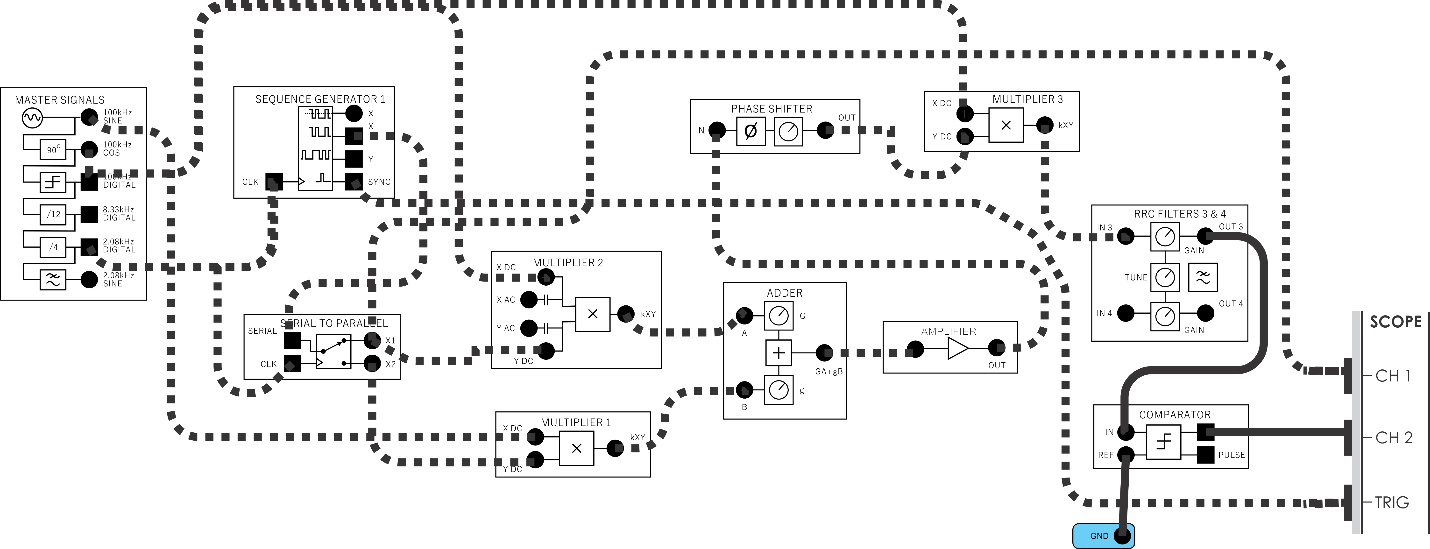


Figure 14: Patching for demodulation of one BPSK channel with comparator digital clean up

The addition of the Comparator module can be represented by the block diagram in Figure 15. If you compare this block diagram with Figure 2 in the preliminary discussion, you’ll notice that this change completes one arm of a QPSK demodulator.

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| 10. | Set the Phase Shifter module’s knob to the fully counterclockwise position. |

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| 11. | Adjust the Phase Shifter module’s knob slowly clockwise until you have recovered the even data bits without any inversion and ignoring any phase shift. |

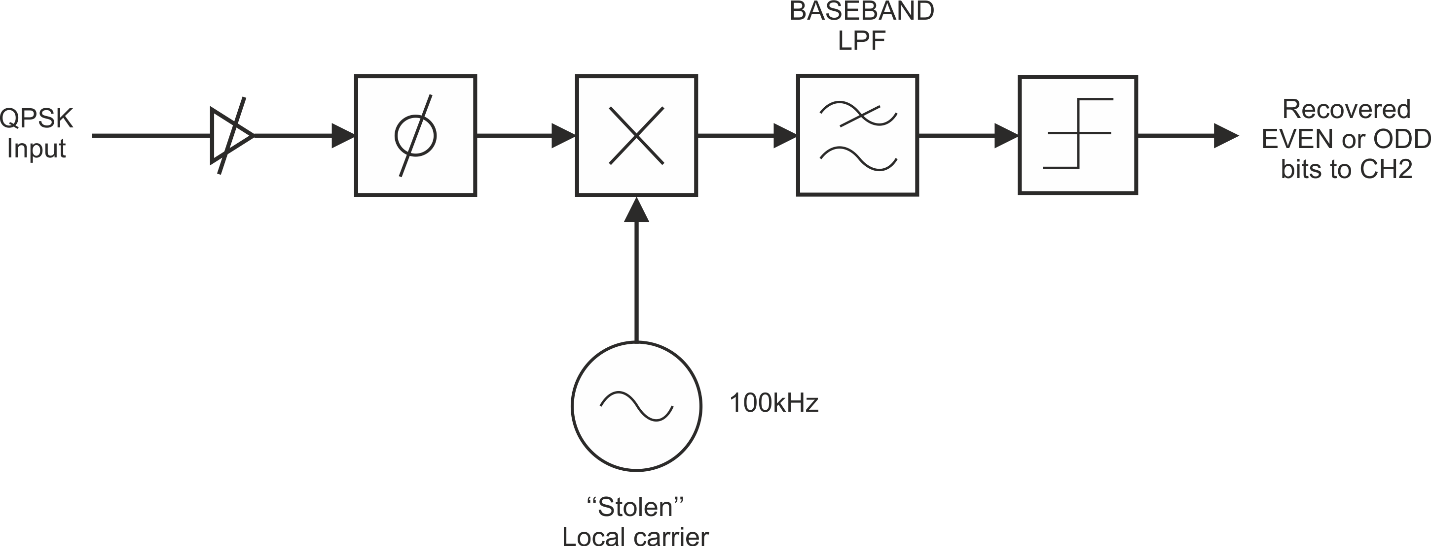


Figure 15: Block diagram for demodulation of one BPSK channel with comparator digital clean up

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| --- | --- |
| 12. | Click the Scope Single button to pause the scope display and compare the even data bits on the Serial-to-Parallel Converter module’s *X1* output (Scope CH 1) with the data on the output of the Comparator module (Scope CH 2). |

3-2 What is the phase relationship between the local carrier and the carrier signals used to generate the PSKI and PSKQ signals?

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| 13. | Unplug Scope CH 1 from the Serial-to-Parallel Converter module’s *X1* output and connect it to the Serial-to-Parallel Converter module’s *X2* output to view the odd data bits. |

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| 14. | Click the Scope Single button to pause the scope display and compare the odd data bits with the recovered data found on the output of the Comparator. They should be different. |

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| 15. | On the Master Signals module, swap the leads coming from the 100kHz SINE output with the leads coming from the 100kHz COS output. |

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| 16. | Click the Scope Single button to pause the scope display and see if the recovered odd data bits on Scope CH 2 match the input odd data bits on Scope CH 1. You may have to adjust the Phase Shifter module’s knob slightly until the odd data bits appear with the correct polarity and ignoring any phase shift. |

3-3 What is the new phase relationship between the local carrier and the carrier signals used to generate the PSKI and PSKQ signals?

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3-4 Why is your demodulator considered to be only one half of a full QPSK receiver?

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| 17. | On the Master Signals module, swap the leads coming from the 100kHz SINE output and the leads coming from the 100kHz COS output to return them to their original position. |

## Section 4: Full QPSK demodulation with data demultiplexing

To this point, you have built a QPSK modulator and demodulated one of the BPSK signals that make up the QPSK signal. You will now build full QPSK demodulator that uses phase discriminators to demodulate both the PSKI and PSKQ channels and then recombines them using a 2-bit Parallel-to-Serial converter.

Figure 16 shows the block diagram of the implementation of the QPSK demodulator you will build.

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|  | **Note**: The 2-bit Parallel-to-Serial converter module includes built-in comparators and so can output a clean digital signal. As such, a separate Comparator as was used in the previous section is not necessary. |

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| 1. | Start with the wiring that you have completed in the previous section and remove the patch cables that connect to the Comparator module. Using this configuration as a starting point, complete the remaining wiring as shown on Figure 17.  **Note:** The Parallel to Serial module *X1* and *X2* inputs should be approximately equal at approximately 4Vpp each. We will now balance the inputs by turning the *GAIN* knobs on the RRC FILTER 3 and RRC FILTER 4 modules. |

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| 2. | Plug Scope CH 1 into the Parallel to Serial module *X1* input. Change the Scope Time per division setting to 20ms. |

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| 3. | With the Scope running, examine the Scope Volts peak – peak measurement for Channel 1. Starting with the RRC FILTER 3 module *GAIN* knob turned fully counterclockwise, slowly turn the RRC FILTER 3 module *GAIN* knob clockwise until the Scope Volts peak – peak measurement is approximately 4.0V. |

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| 4. | Plug Scope CH 1 into the Parallel to Serial module *X2* input. With the Scope running, examine the Scope Volts peak – peak measurement for Channel 1. Starting with the RRC FILTER 4 module *GAIN* knob turned fully counterclockwise, slowly turn the RRC FILTER 4 module *GAIN* knob clockwise until the Scope Volts peak – peak measurement is approximately 4.0V. |

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| 5. | Plug Scope CH 1 into the Sequence Generator 1 module Unipolar *X* output. Plug Scope CH 2 into the Parallel to Serial module *SERIAL* output. |
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| 6. | Turn the Parallel to Serial module *ALIGN* knob fully counter clockwise. |

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| 7. | Change the Scope Time per division setting to 1ms. Compare the recovered bits (Scope CH 2) to the original bits (Scope CH 1). |

At first glance, these two signals appear to be different when they should be the same. Can you work out what’s going on? **Tip:** Vertically offset the two data sequences so that one appears above the other in the display. Vary the Scope Time per division setting a bit to see different lengths of the two data sequences.

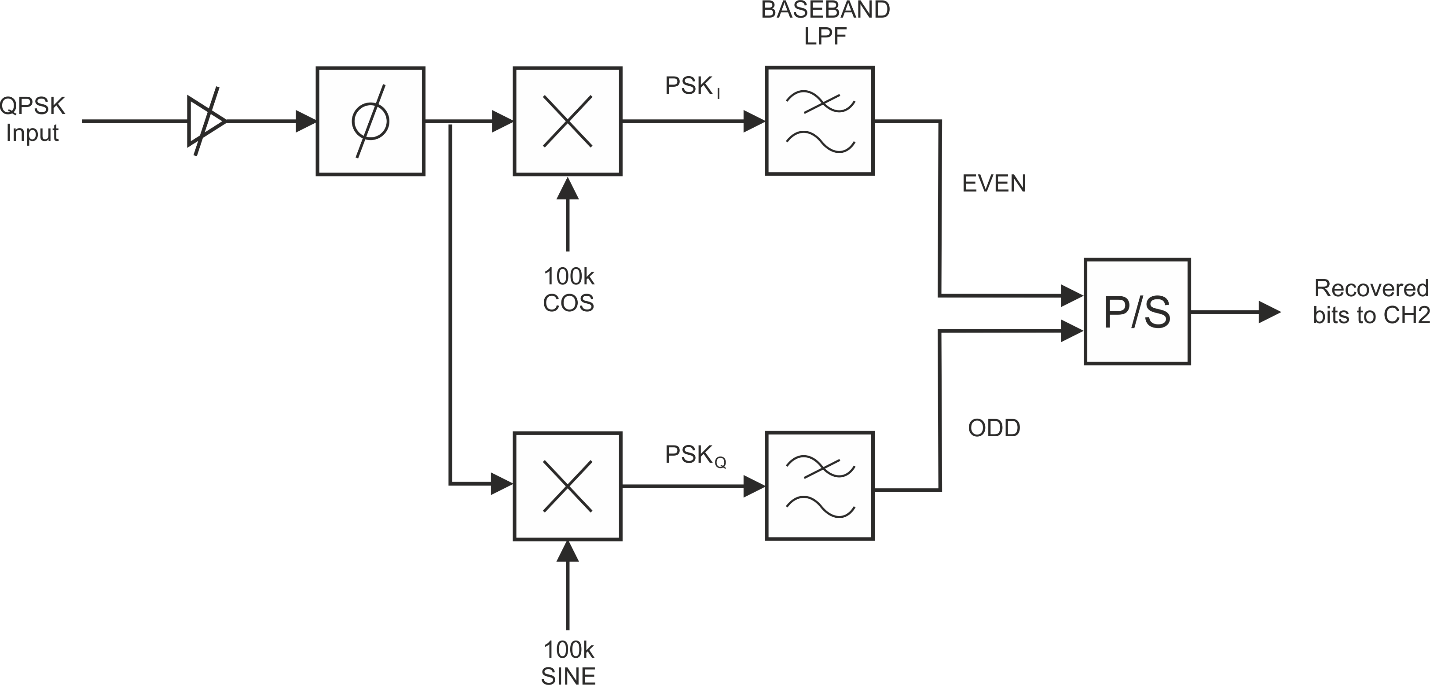
**

Figure 16: Block diagram for full QPSK demodulation

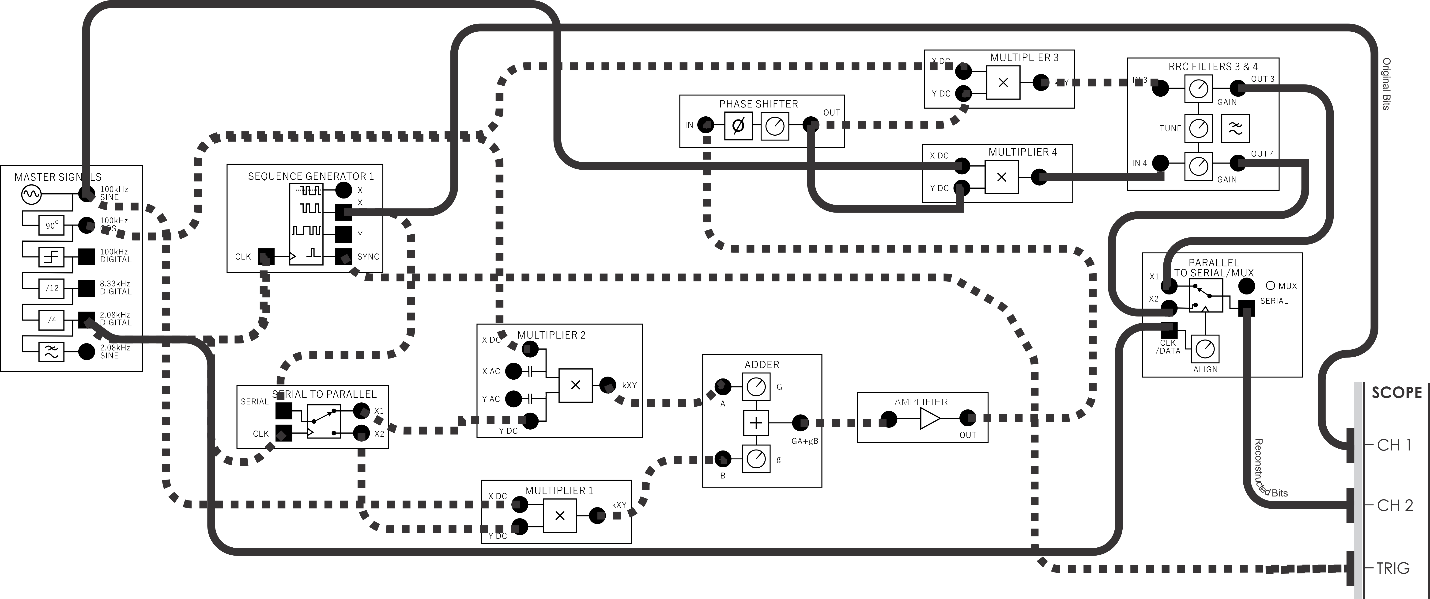


Figure 17: Patching for full QPSK demodulation

4-1 Are the generated and recovered data signals the same? Explain your answer.

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## Section 5: Constellation view of the recovered I/Q signals

For another perspective on the recovery of the even and odd data signals, which are usually referred to as I & Q signals, if we view these signals out of the dual baseband LPF’s at the same time and when the phase is adjusted for correct recovery, we see that each signal has only two levels.

Viewing these two signals in XY mode on a Scope will display these more or less as a square shape known as a “constellation”. This “constellation” has 4 points, one for each possible combination of the two signals ie: 2 signals x 2 levels = 4 points.

If the Phase is NOT adjusted correctly, then each signal will have more than two levels and the constallation will appear rotated. Try experimenting with varying the phase and aim to understand why this causes the constallation to rotate.

Think about what DC levels would be required to create points which are not symetrical about the X & Y axis and relate this back to the I & Q signals.

In Figure 18, The “corners” or “points” of the constellation are the periods when both I & Q signals are at a constant DC level. For example, when both signals are at +2V, then the constellation creates a point at (+2V, +2V) and so on for the other 3 points.

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| Figure 18: Example of a Constellation view for several Phase positions |  |

A more insightful way of viewing quadrature signals is known as the “Constellation viewer” which is simply an XY mode display with persistence ie: the overlay of multiple bit periods of BOTH I & Q signals over a period of time with persistance.

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| 1. | Launch the supplied instrument “ECB\_EYE\_BER\_CONSTELLATION viewer” by running the file “ECB\_EYE\_BER\_CONSTELLATION viewer\_LV2018”. You will need to “stop” the ELVIS III scope instrument as the Viewer software uses the scope resources itself. Ensure the scope leads are connected as per Figure 5. |

The viewer software has 2 tabs.

1) EYE & BER

2) CONSTELLATION

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| 1. | Select the CONSTELLATION tab and connect scope Channel 1 and Channel 2 to inputs X1 and X2 of the PARALLEL to SERIAL module respectively.  Once you have the instrument running you can view the recovered signal in the time domain as well as in a constellation. You may wish to change the Total Acquisition Time to 0.01 to capture more periods. As well you can change the “max captures” value to a lower value eg. 5, so that you can see the changes more easily. |

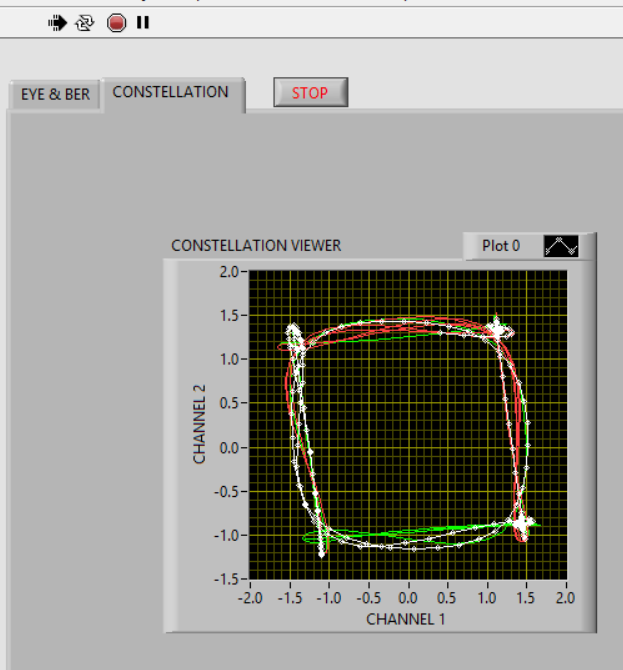


Figure 19: Constellation view of I/Q signals